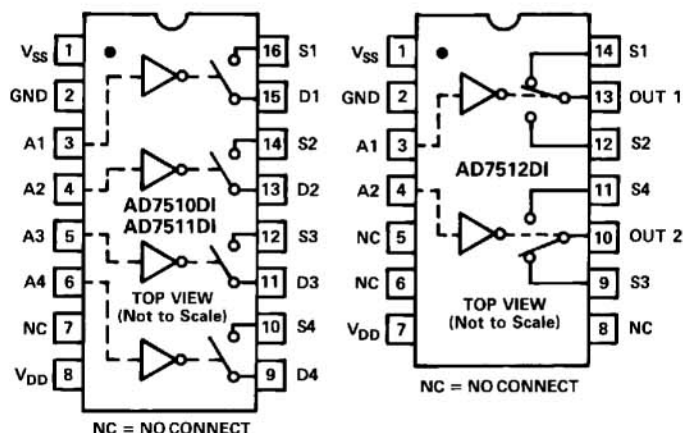


**AD7510DI/AD7511DI/AD7512DI**
**FEATURES**
**Latch-Proof**
**Overvoltage-Proof:  $\pm 25V$** 
**Low  $R_{ON}$ :  $75\Omega$** 
**Low Dissipation: 3mW**
**TTL/CMOS Direct Interface**
**Silicon-Nitride Passivated**
**Monolithic Dielectrically-Isolated CMOS**
**Standard 14-/16-Pin DIPs and**
**20-Terminal Surface Mount Packages**
**DIP FUNCTIONAL DIAGRAMS**

**GENERAL DESCRIPTION**

The AD7510DI, AD7511DI and AD7512DI are a family of latch proof dielectrically isolated CMOS switches featuring overvoltage protection up to  $\pm 25V$  above the power supplies. These benefits are obtained without sacrificing the low "ON" resistance ( $75\Omega$ ) or low leakage current ( $500pA$ ), the main features of an analog switch.

The AD7510DI and AD7511DI consist of four independent SPST analog switches packaged in either a 16-pin DIP or a 20-terminal surface mount package. They differ only in that the digital control logic is inverted. The AD7512DI has two independent SPDT switches packaged either in a 14-pin DIP or a 20-terminal surface mount package.

Very low power dissipation, overvoltage protection and TTL/CMOS direct interfacing are achieved by combining a unique circuit design and a dielectrically isolated CMOS process. Silicon nitride passivation ensures long term stability while monolithic construction provides reliability.

**CONTROL LOGIC**

AD7510DI: Switch "ON" for Address "HIGH"

AD7511DI: Switch "ON" for Address "LOW"

AD7512DI: Address "HIGH" makes S1 to Out 1 and S3 to Out 2

**ORDERING GUIDE**

Model <sup>1</sup>	Temperature Range	Package Option <sup>2</sup>
AD7510DIKN	0 to +70°C	N-16
AD7510DIKP	0 to +70°C	P-20A
AD7510DIKQ	-25°C to +85°C	Q-16
AD7510DISQ	-55°C to +125°C	Q-16
AD7510DISE	-55°C to +125°C	E-20A
AD7511DIKN	0 to +70°C	N-16
AD7511DIKP	0 to +70°C	P-20A
AD7511DIKQ	-25°C to +85°C	Q-16
AD7511DISQ	-55°C to +125°C	Q-16
AD7511DITE	-55°C to +125°C	E-20A
AD7512DIKN	0 to +70°C	N-14
AD7512DIKP	0 to +70°C	P-20A
AD7512DIKQ	-25°C to +85°C	Q-14
AD7512DITQ	-55°C to +125°C	Q-14
AD7512DITE	-55°C to +125°C	E-20A

**NOTES**

<sup>1</sup>To order MIL-STD-883, Class B, processed parts, add/883B to part number. See Analog Devices Military Products Databook (1990) for military data sheet.

<sup>2</sup>E = Leadless Ceramic Chip Carrier (LCCC); N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip.

**REV. A**

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# AD7510DI/AD7511DI/AD7512DI — SPECIFICATIONS

( $V_{DD} = +15V$ ,  $V_{SS} = -15V$ , unless otherwise noted.)

## INDUSTRIAL VERSION (K)

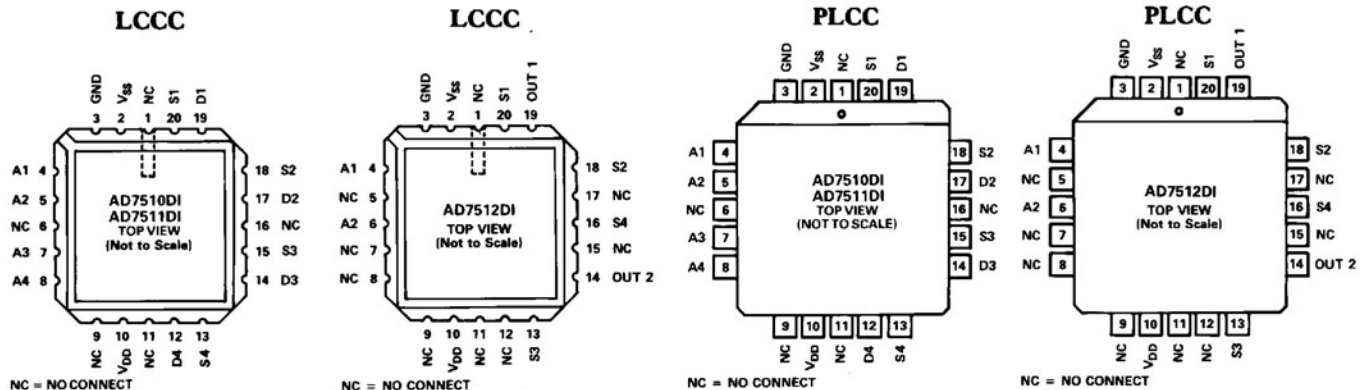
PARAMETER	MODEL	VERSION	+25°C (N, P, Q)	0 to +70°C (N, P) -25°C to +85°C (Q)	TEST CONDITIONS
<b>ANALOG SWITCH</b>					
$R_{ON}^1$	All	K	75Ω typ, 100Ω max	175Ω max	$-10V \leq V_D \leq +10V$ $I_{DS} = 1.0mA$
$R_{ON}$ vs $V_D$ ( $V_S$ )	All	K	20% typ		
$R_{ON}$ Drift	All	K	+0.5%/°C typ		$V_D = 0$ , $I_{DS} = 1.0mA$
$R_{ON}$ Match	All	K	1% typ		
$R_{ON}$ Drift Match	All	K	0.01%/°C typ		
$I_D$ ( $I_S$ )OFF <sup>1</sup>	All	K	0.5nA typ, 5nA max	500nA max	$V_D = -10V$ , $V_S = +10V$ and $V_D = +10V$ , $V_S = -10V$
$I_D$ ( $I_S$ )ON <sup>1</sup>	All	K	10nA max		$V_S = V_D = +10V$ $V_S = V_D = -10V$
$I_{OUT}^1$	AD7512DI	K	15nA max	1500nA max	$V_{S1} = V_{OUT} = \pm 10V$ , $V_{S2} = \mp 10V$ and $V_{S2} = V_{OUT} = \pm 10V$ , $V_{S1} = \mp 10V$
<b>DIGITAL CONTROL</b>					
$V_{INL}^1$	All	K		0.8V max	
$V_{INH}^1$	All	K		2.4V min	
$C_{IN}$	All	K	7pF typ		
$I_{INH}^1$	All	K	10nA max		$V_{IN} = V_{DD}$
$I_{INL}^1$	All	K	10nA max		$V_{IN} = 0$
<b>DYNAMIC CHARACTERISTICS</b>					
$t_{ON}$	AD7510DI	K	180ns typ		$V_{IN} = 0$ to +3.0V
	AD7511DI	K	350ns typ		
$t_{OFF}$	AD7510DI	K	350ns typ		
	AD7511DI	K	180ns typ		
$t_{TRANSITION}$	AD7512DI	K	300ns typ		
$C_S$ ( $C_D$ )OFF	All	K	8pF typ		$V_D$ ( $V_S$ ) = 0V
$C_S$ ( $C_D$ )ON	All	K	17pF typ		
$C_{DS}$ ( $C_{S-OUT}$ )	All	K	1pF typ		
$C_{DD}$ ( $C_{SS}$ )	All	K	0.5pF typ		
$C_{OUT}$	AD7512DI	K	17pF typ		
$Q_{INJ}$	All	K	30pC typ		
<b>POWER SUPPLY</b>					
$I_{DD}^1$	All	K	800μA max	800μA max	All digital inputs = $V_{INH}$
$I_{SS}^1$	All	K	800μA max	800μA max	
$I_{DD}^1$	All	K	500μA max	500μA max	All digital inputs = $V_{INL}$
$I_{SS}^1$	All	K	500μA max	500μA max	

### NOTES

<sup>1</sup> 100% tested.

Specifications subject to change without notice.

## PIN CONFIGURATIONS



## EXTENDED VERSIONS (S, T)

PARAMETER	MODEL	VERSION	+25°C	-55°C to +125°C	TEST CONDITIONS
<b>ANALOG SWITCH</b>					
$R_{ON}^1$	All	S, T	100Ω max	175Ω max	$-10V \leq V_D \leq +10V$ $I_{DS} = 1mA$
$I_D (I_S)_{OFF}^1$	All	S, T	3nA max	200nA max	$V_D = -10V, V_S = +10V$ and $V_D = +10V, V_S = -10V$
$I_D (I_S)_{ON}^1$	All	S, T	10		$V_S = V_D = +10V$ and $V_S = V_D = -10V$
$I_{OUT}^1$	AD7512DI	S, T	9nA max	600nA max	$V_{S1} = V_{OUT} = \pm 10V$ $V_{S2} = \mp 10V$ and $V_{S2} = V_{OUT} = \pm 10V$ $V_{S1} = \mp 10V$
<b>DIGITAL CONTROL</b>					
$V_{INL}^1$	All	S, T		0.8V max	
$V_{INH}^{1,2}$	AD7510DI	S		2.4V min	
	AD7511DI	T		2.4V min	
	AD7512DI	T		2.4V min	
	AD7511DI	S		3.0V min	
	AD7512DI	S		3.0V min	
$I_{INH}^1$	All	S, T	10nA max		$V_{IN} = V_{DD}$
$I_{INL}^1$	All	S, T	10nA max		$V_{IN} = 0$
<b>DYNAMIC CHARACTERISTICS</b>					
$t_{ON}^3$	AD7510DI	S,	1.0μs max		$V_{IN} = 0$ to +3V
	AD7511DI	S, T	1.0μs max		
$t_{OFF}^3$	AD7510DI	S, T	1.0μs max		
	AD7511DI	S, T	1.0μs max		
$t_{TRANSITION}^3$	AD7512DI	S, T	1.0μs max		
<b>POWER SUPPLY</b>					
$I_{DD}^1$	All	S, T		800μA max	All digital inputs = $V_{INH}$
$I_{SS}^1$	All	S, T		800μA max	
$I_{DD}^1$	All	S, T		500μA max	All digital inputs = $V_{INL}$
$I_{SS}^1$	All	S, T		500μA max	

**NOTES**

<sup>1</sup> 100% tested.

<sup>2</sup> A pullup resistor, typically 1-2kΩ is required to make AD7511DISQ and AD7512DISQ TTL compatible.

<sup>3</sup> Guaranteed, not production tested.

Specifications subject to change without notice.

**ABSOLUTE MAXIMUM RATINGS\***

$V_{DD}$  to GND . . . . . +17V

$V_{SS}$  to GND . . . . . -17V

Overvoltage at  $V_D (V_S)$

(1 second surge) . . . . .  $V_{DD} + 25V$   
or  $V_{SS} - 25V$

(Continuous) . . . . .  $V_{DD} + 20V$   
or  $V_{SS} - 20V$

or 20mA, Whichever Occurs First

Switch Current ( $I_{DS}$ , Continuous) . . . . . 50mA

Switch Current ( $I_{DS}$ , Surge)

1ms Duration, 10% Duty Cycle . . . . . 150mA

Digital Input Voltage Range . . . . . 0V to  $V_{DD} + 0.3V$

Power Dissipation (Any Package)

Up to +75°C . . . . . 450mW

Derates above +75°C by . . . . . 6mW/°C

Lead Temperature (Soldering, 10sec) . . . . . +300°C

Storage Temperature . . . . . -65°C to +150°C

Operating Temperature

Commercial (KN, KP Versions) . . . . . 0 to +70°C

Industrial (KQ Versions) . . . . . -25°C to +85°C

Extended (SQ, TQ, SE, TE Versions) . . . . . -55°C to +125°C

\*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

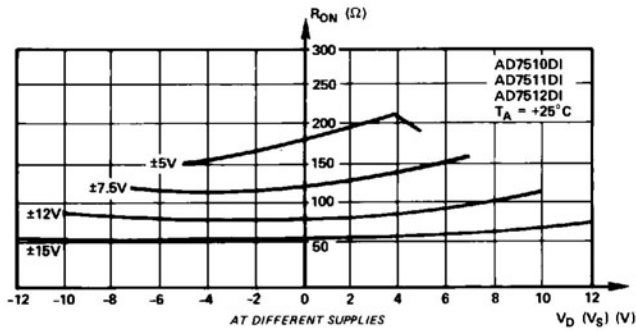
**CAUTION**

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

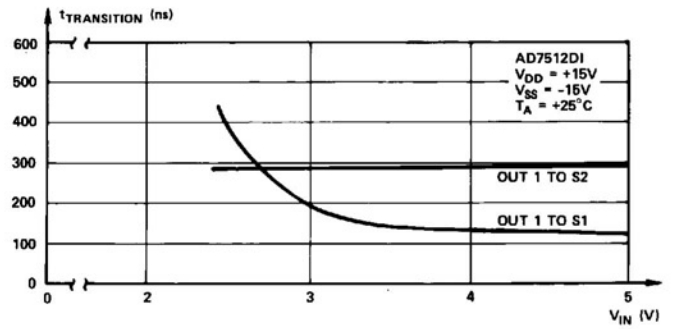




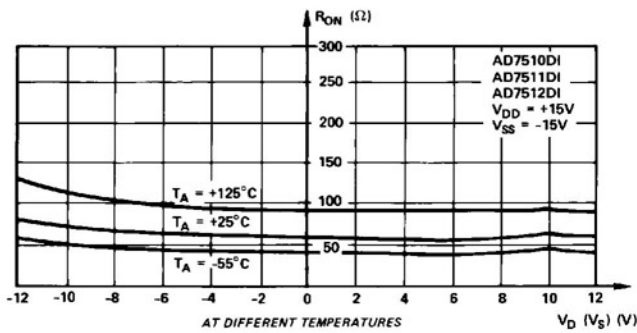
# Typical Performance Characteristics—AD7510DI/AD7511DI/AD7512DI



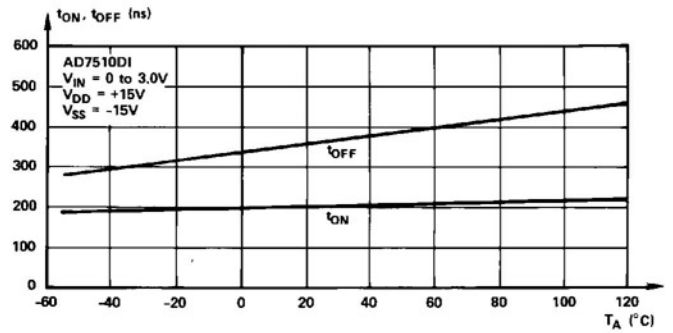
$R_{ON}$  as a Function of  $V_D$  ( $V_S$ )



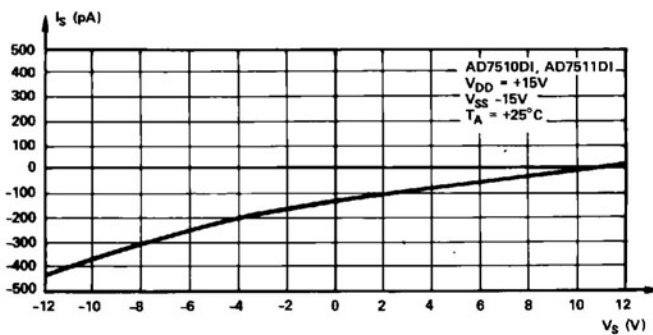
$t_{TRANSITION}$  as a Function of Digital Input Voltage



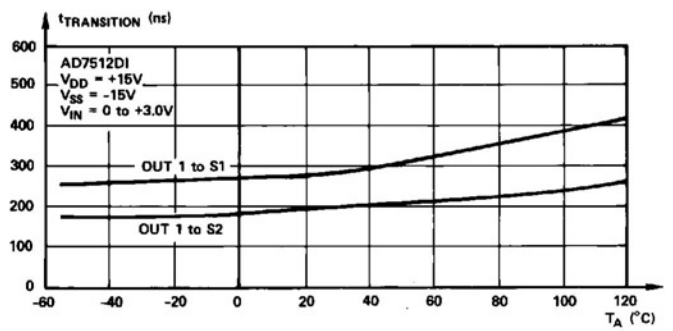
$R_{ON}$  as a Function of  $V_D$  ( $V_S$ )



$t_{ON}$ ,  $t_{OFF}$  as a Function of Temperature



$I_S$ , ( $I_D$ )<sub>OFF</sub> vs  $V_S$

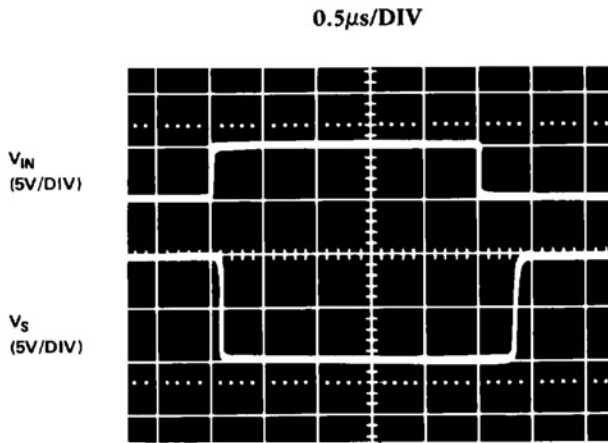


$t_{TRANSITION}$  as a Function of Temperature

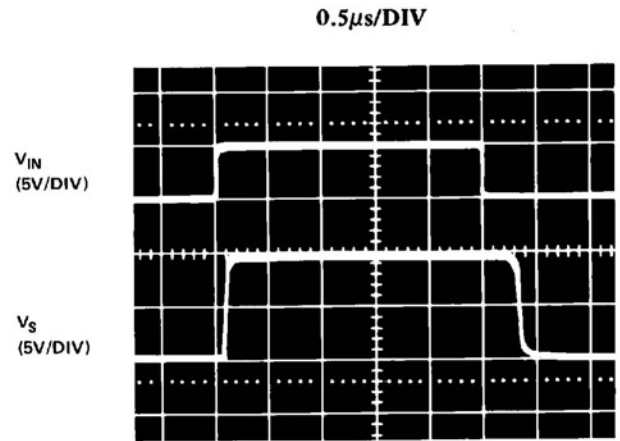
# AD7510DI/AD7511DI/AD7512DI

## TYPICAL SWITCHING CHARACTERISTICS

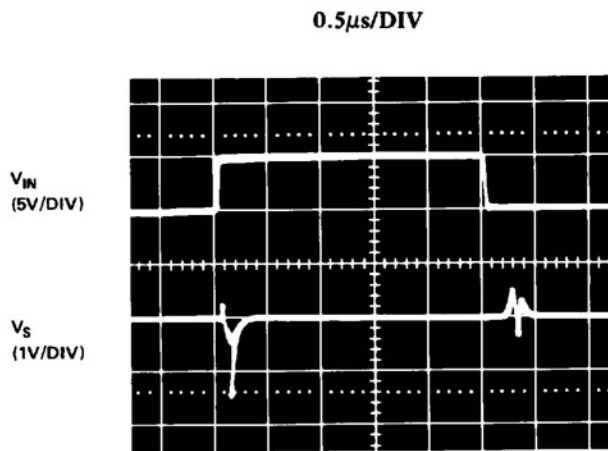
## AD7510DI, AD7511DI



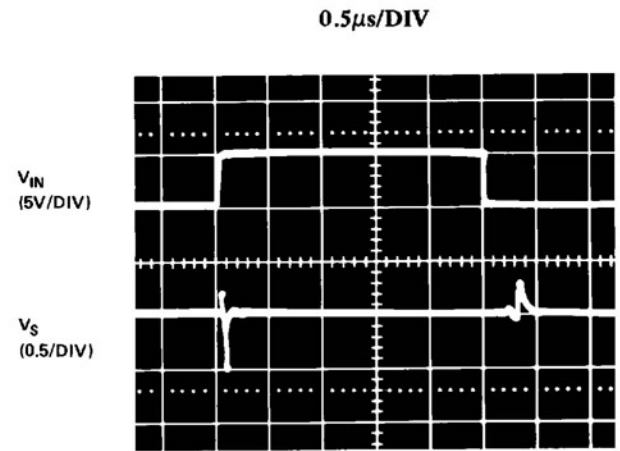
Switching Waveforms for  $V_D = -10V$



Switching Waveforms for  $V_D = +10V$

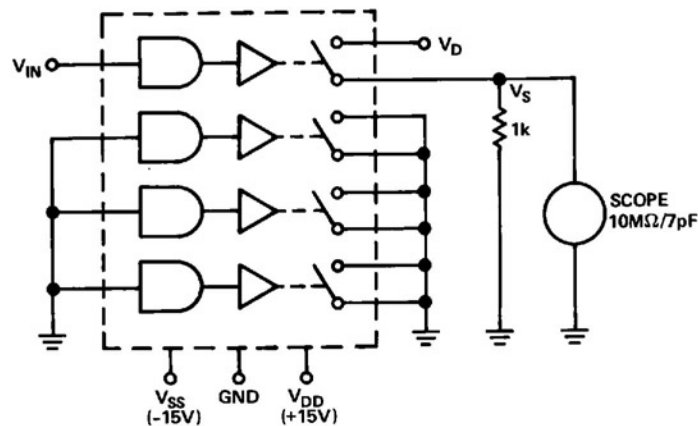


Switching Waveforms for  $V_D = \text{Open}$



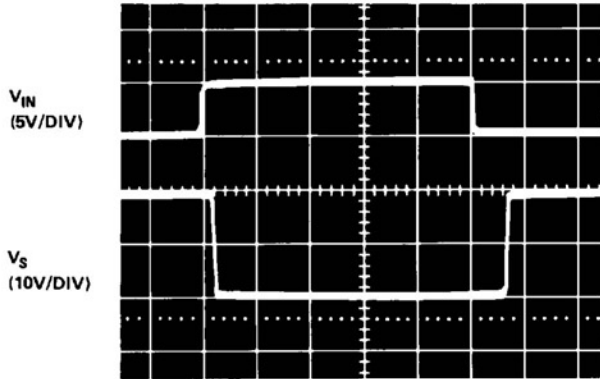
Switching Waveforms for  $V_D = 0V$

### AD7510DI, AD7511DI TEST CIRCUIT



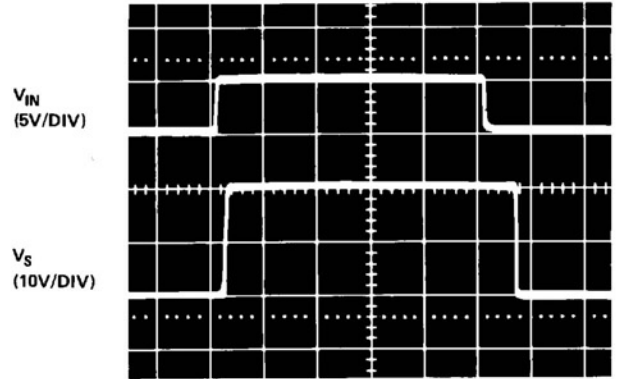
AD7512DI

0.5μs/DIV



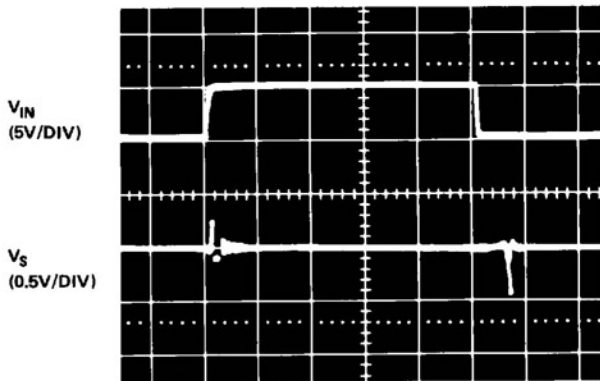
Switching Waveforms for  $V_{S1} = -10V$ ,  $V_{S2} = +10V$ ,  $R_L = 1k$

0.5μs/DIV



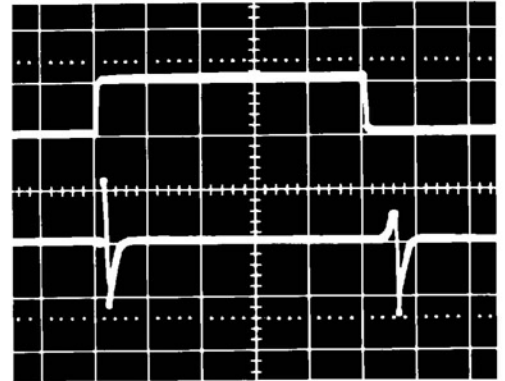
Switching Waveforms for  $V_{S1} = +10V$ ,  $V_{S2} = -10V$ ,  $R_L = \infty$

0.5μs/DIV



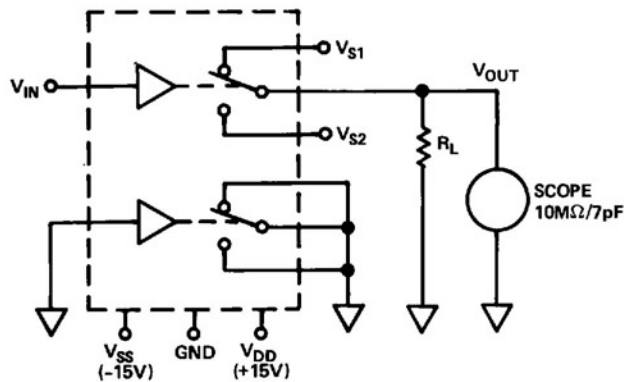
Switching Waveforms for  $V_{S1}$  and  $V_{S2} = 0V$ ,  $R_L = \infty$

0.5μs/DIV



Switching Waveforms for  $V_{S1}$  and  $V_{S2} = \text{Open}$ ,  $R_L = 1k$

AD7512DI TEST CIRCUIT



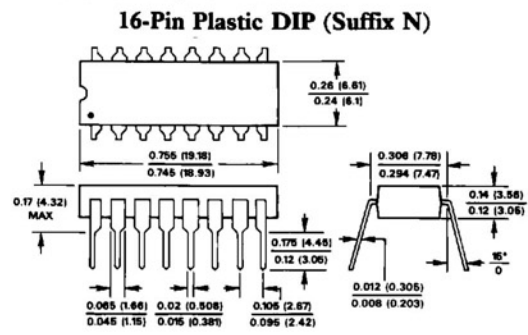
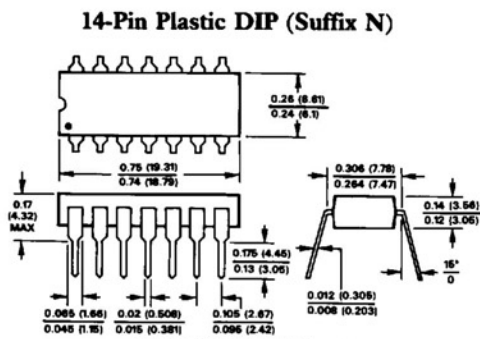
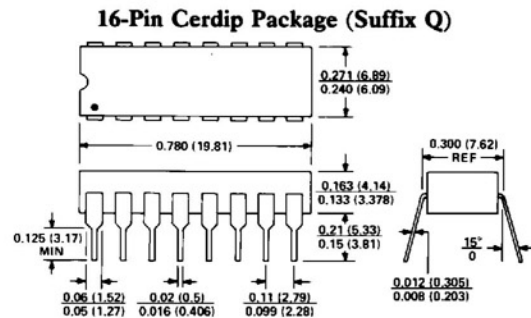
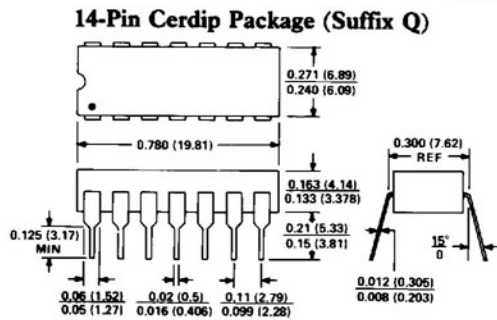
# AD7510DI/AD7511DI/AD7512DI

## TERMINOLOGY

$R_{ON}$	Ohmic resistance between terminals D and S.	$C_{DD} (C_{SS})$	Capacitance between terminals D (S) of any two switches. (This will determine the cross coupling between switches vs. frequency.)
$R_{ON}$ Drift Match	Difference between the $R_{ON}$ drift of any two switches.	$t_{ON}$	Delay time between the 50% points of the digital input and switch "ON" condition.
$R_{ON}$ Match	Difference between the $R_{ON}$ of any two switches.	$t_{OFF}$	Delay time between the 50% points of the digital input and switch "OFF" condition.
$I_D (I_S)_{OFF}$	Current at terminals D or S. This is a leakage current when the switch is "OFF".	$t_{TRANSITION}$	Delay time when switching from one address state to another.
$I_D (I_S)_{ON}$	Leakage current that flows from the closed switch into the body. (This leakage will show up as the difference between the current $I_D$ going into the switch and the outgoing current $I_S$ .)	$V_{INL}$	Maximum input voltage for a logic low.
$V_D (V_S)$	Analog voltage on terminal D (S).	$V_{INH}$	Minimum input voltage for a logic high.
$C_S (C_D)$	Capacitance between terminal S (D) and ground. (This capacitance is specified for the switch open and closed.)	$I_{INL} (I_{INH})$	Input current of the digital input.
$C_{DS}$	Capacitance between terminals D and S. (This will determine the switch isolation over frequency.)	$C_{IN}$	Input capacitance to ground of the digital input.
		$V_{DD}$	Most positive voltage supply.
		$V_{SS}$	Most negative voltage supply.
		$I_{DD}$	Positive supply current.
		$I_{SS}$	Negative supply current.

## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



**20-Terminal Leadless Ceramic Chip Carrier (Suffix E)**

